REMARKS

Claims 1-12, 14-16 and 18-22 are all the claims presently pending in the application. Claims 1, 5, 1, 14, 16, 18 and 20 have been amended to more particularly define the invention. Claims 21-22 have been added to claim additional features of the claimed invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicant gratefully acknowledges that claims 11, 16 and 20 would be allowed if rewritten in independent form. Applicant notes that claims 11, 16 and 20 have been rewritten in independent form and are thus, in condition for immediate allowance.

Claims 1-10, 12, 14-15 and 18-19 stand rejected under 35 USC 103(a) as unpatentable over Kataoka et al. (US Pat. No. 6,266,111) in view of Rho et al. (US Pat. No. 6,057,896).

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as defined by claim 1) is directed to a liquid crystal display device, including a plurality of pixels arranged in a matrix form. Each of the pixels includes a pixel electrode formation area wherein a pixel electrode is formed, and a thin film transistor formation area wherein a thin film transistor is formed and connected to the pixel electrode.

Further, the thin film transistor includes a semiconductor layer serving as a channel, a terminal formed to be connected to the pixel electrode, an inorganic insulating passivation layer formed to cover the thin film transistor, and a transparent organic insulating layer covering the passivation layer.

In another aspect (e.g., as defined by claim 14 and similarly defined in the method of claim 18), the claimed invention is directed to a thin film transistor array substrate for a liquid crystal display device, the substrate includes an insulating substrate; a plurality of data lines formed on the insulating substrate; a plurality of gate lines formed on the insulating substrate,

such that areas bounded by the plurality of gate lines and the plurality of data lines define a plurality of pixels in the liquid crystal display device; a plurality of thin film transistors respectively formed on the insulating substrate in the plurality of pixels; a plurality of prism-shaped base posts formed adjacent to a thin film transistor in each of the plurality of pixels; an uneven layer formed on the plurality of prism-shaped base posts, the uneven layer comprising a transparent organic insulating layer; and a pixel electrode formed on the uneven layer. Further, the thin film transistor includes a gate insulation layer formed on the transparent insulating substrate, a semiconductor layer formed on the gate insulation layer, and an inorganic passivation layer formed on the semiconductor layer.

Conventional liquid crystal displays have attempted to improve performance by forming uneven layers using an organic insulating layer on an active matrix substrate and forming a reflection electrode thereon (Application at page 6, lines 1-5). However, such attempts complicate the manufacturing steps and decrease productivity (Application at page 7, lines 15-20).

An aspect of the claimed invention, on the other hand, includes a thin film transistor including an inorganic insulating passivation layer formed to cover the thin film transistor, and a transparent organic insulating layer covering the passivation layer (Application at page 20, lines 21-26; Figure 7A). This passivation layer may be used for example, for planarizing. Another aspect of the claimed invention includes an uneven layer formed on the plurality of prism-shaped base posts, the uneven layer including a transparent organic insulating layer (Application at page 25, lines 9-13; Figures 11A-11B). These features allow the claimed invention to require fewer manufacturing steps than conventional devices (Application at page 27, lines 16-24).

II. THE KATAOKA AND RHO REFERENCES

The Examiner alleges that Kataoka would have been combined with Rho to form the claimed invention. Applicant submits, however, that these references would not have been combined, and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Kataoka discloses a diffuse reflection plate which includes a substrate, resin prisms formed on the substrate, a metal film formed on the prisms, a curved resin film between the

prisms, and a plurality of thin film transistors on the surface of the substrate, the transistors including gate electrodes, insulating films on the gate electrodes, a thin film on insulating film, and a channel region formed on the thin film (Kataoka at col. 8, line 60-col. 9, line 20).

Rho discloses a liquid crystal display in which a passivation layer is formed by coating a flowable insulating material on the substrate where a thin film transistor and a storage capacitor electrode, and a pixel electrode is formed on the passivation layer. A portion of the passivation layer is etched using the pixel electrode as a mask to make a groove on the thin film transistor, and then a black matrix is formed by filling an organic black photoresist in the groove (Rho at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions. Indeed, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, Applicant notes that the Examiner has failed to support the alleged combination with specific suggestions or motivation from any of the references. In fact, Applicant respectfully submits that there is no such motivation or suggestion to combine the references, and one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Kataoka, nor Rho, nor any combination thereof teaches or suggests a liquid crystal display device having pixels with transistors which include "*an inorganic insulating passivation layer formed to cover said thin film transistor; and a transparent organic insulating layer covering said passivation layer*", as recited, for example, in claim 1, nor "*an uneven layer formed on said plurality of prism-shaped base posts, said uneven layer comprising a transparent organic insulating layer*", as recited, for example, in claim 14 and similarly recited in claim 18.

As noted above, unlike conventional liquid crystal displays which require complicated manufacturing steps and are associated with a decreased productivity, the claimed invention includes an inorganic insulating passivation layer formed to cover the thin film transistor,

and a transparent organic insulating layer covering the passivation layer, in one aspect, and an uneven layer formed on the plurality of prism-shaped base posts, the uneven layer including a transparent organic insulating layer in another aspect (Application at page 25, lines 9-13; Figures 11A-11B). These features allow the claimed invention to require fewer manufacturing steps than conventional devices (Application at page 27, lines 16-24).

Clearly, these features are not taught or suggested by any of the cited references. Indeed, Applicant points out that the Examiner expressly concedes that these features are not taught or suggested by Kataoka (e.g., see Office Action at paragraph 4, page 2). The Examiner alleges that these features are taught by Rho. However, the Examiner is clearly incorrect.

In fact Applicant points out to the Examiner that the passivation layer 100 of Figure 3 in Rho consists of an organic material and is different from a passivation film 28 made of an inorganic insulating layer, as shown in Figure 7A of the present Application. Moreover, an organic layer 110 of Figure 3 in Rho is not transparent and is used as black matrix. On the other hand, an organic insulating layer 29 covering a passivation film 28 as shown in Figure 7A in the present Application is transparent and can be used for planarizing. The organic insulating layer 29 may include a transparent acrylic resin etc. as described on page 20, lines 21-26 of the present Application.

Further, the passivation film 28 which is illustrated in Figure 7A of the present Application includes (e.g., consists of) an inorganic insulating layer such as a silicon nitride film as described on page 19, lines 19-20 of the present Application, and is clearly different from the passivation layer 100 in Rho, which is made of an organic material.

In addition, the passivation film 28 is illustrated in Figures 11A and 11B of the present Application. An unevenness layer 39 which includes a thick film is also illustrated in Figures 11A and 11B of the present Application. The unevenness layer 39 covering the passivation film 28 may include (e.g., consist of) a transparent acrylic resin, as described on page 25, lines 9-13 of the present Application.

Thus, like Kataoka, Rho does not teach or suggest the novel features of the claimed invention. Indeed, nowhere does Rho teach or suggest a thin film transistor including an inorganic insulating passivation layer formed to cover the thin film transistor, and a transparent organic insulating layer covering the passivation layer. Thus, Rho does not make

up for the deficiencies of Kataoka.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-12, 14-16 and 18-22, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 10/13/04

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Fazli Erdem, Group Art Unit # 2826 at fax number (703) 872-9306 this 13th day of October, 2004.

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